REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

By the foregoing amendment, claims 1, 3, and 23 have been amended. Claims 2 and 4 were previously canceled. No new matter has been added. Thus, claims 1, 3, 5-12, and 23 are currently pending in this application and subject to examination.

In the Office Action mailed January 19, 2006, the Examiner rejected claims 1, 3, 5-11, and 23 under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner rejected claims 1, 3, and 4-12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,928,208 to Kokubo et al. ("Kokubo"). The Examiner did not state that claim 23 was rejected as being anticipated by Kokubo. However, the Applicants assume this was a mistake as the rejection includes a description of Kokubo's teachings in reference to claim 23. The Applicants hereby traverse the rejection as follows.

The Applicants thank the Examiner for noting that claim 5 would be allowable over the cited art. Claim 5 was listed as being rejected as anticipated by Kokubo on page 3 under the citation of 35 U.S.C. § 102(b), however, there is no description of how claim 5 is anticipated by the cited art. As claim 5 is described in the Allowable Subject Matter section as distinguishing the cited art, we assume that claim 5 is not rejected under 35 U.S.C. § 102(b).

I. Rejections under 35 U.S.C. § 112

In the Office Action mailed January 19, 2006, the Examiner rejected claims 1, 3, 5-11, and 23 under 35 U.S.C. § 112, second paragraph as being indefinite. The Applicants respectfully traverse this rejection.

A. "the counter, the subtracter . . .succeeding counting period"

Regarding the expression in claim 1 that "the counter, the subtracter . . . having characteristics such that when the count value is changed from a preceding count value, the frequency of the output clock signal is changed during a period in which the reference clock signal is a Low level, after the end of the counting period and before the start of a succeeding counting period" in lines 16-20, the Examiner is correct in the understanding that the frequency of output (ST) changes with the analog control voltage (AV). However, this analog control voltage does not always change. The subject matter of claim 1 corresponds to a first embodiment described in the current application and shown in Figures 2 and 3, not Figures 4 and 5, as suggested by the Examiner. In Figure 3, the analog control voltage is shown as changing during the period, between T1 and T2, at which the reference clock signal is at a low level.

The Examiner noted that Figures 3 and 4 of the present invention show the frequency of the output clock signal, ST, changing when the reference clock signal is at both low and high levels. However, as noted above, claim 1 is directed to an embodiment described with respect to Figures 2 and 3, not to Figure 4. Figure 4 corresponds to a second embodiment. Figure 3 consistently shows the output clock signal changing when the reference clock signal is at a low level, as claimed in claim 1 with the language "the frequency of the output clock signal is changed during a period in which the reference clock signal is a Low level."

The specification describes that in order to output an output clock signal obtained by multiplying a reference clock signal, an output clock signal ST is counted by a counter, 2, for a certain period (e. g. in claim 1, during the time that the reference clock

signal is at a high level), a process is performed using the obtained count value, CN, to change the analog control voltage, AV, from a DA converter, DAC. (See page 10, line 20-page 11, line 25 and figure 3). This is associated with the levels, high and low, of the reference clock signal. As in claim 1, figure 3 shows this analog control voltage, AV, is maintained at a value AV1 and changed to another value AV2 at a timing associated with the reference clock signal. Figure 3 also reveals that the analog control voltage, AV, changes at time intervals (not constantly) and the timing of such change is associated with the time at which the reference clock signal is at a low level, consistent with claim 1.

Specifically, a difference value DN1, an integrated vale IN1, and an analog control voltage AV1 are generated in order, as shown in Figure 3. The generation of these values is based on a count value CN1 obtained by counting the output clock signal, ST, during the period at which the reference clock signal, SR, for a High level period, T1. By using the analog control voltage, AV1, the frequency of the output clock signal, ST, to be outputted from VCO7 is changed. The counter, 2, subtracter, 3, control voltage generation circuits, 3 and 4, and VCO7 output: the count value, CN1, difference value, DN1, integrated value, IN1, and analog control voltage, AV1, in order within a low level period of the reference clock signal, SR, to the start of a next High level period, T2, thereof. The frequency of the output clock signal, ST, is changed by the analog control voltage, AV1. With the above configuration, which is reflected in the language cited by the Examiner for claim 1, the present invention can provide an better response. Thus, the Applicants submit that the language in claim 1 is not indefinite.

Although the Examiner did not mention claim 23, claim 23 is directed to an embodiment with an opposite configuration to claim 1. The modified embodiment claimed in claim 23 corresponds to the embodiment depicted in Figures 2 and 4. For similar to reasons to those discussed above for claim 1, the Applicants submit that claim 23 is likewise definite.

B. "integral value of the difference value"

The Applicants submit that the term "integral value of a difference value" is definite, as defined in claim 1 and as the term is described in the specification. Claim 1 recites that the difference value is obtained by subtracting either the count value or a reference value from the other. The integrated value of the difference value represents a value obtained by integration of this difference value, DN, that is, a value obtained by repeated accumulation of the obtained difference value. (See also page 10, lines 1-5). In processing with digital values, integration means repeated sum. As described in the specification, the newly obtained difference value, DN, is added to the integrated value IN generating a new integrated value IN (IN = IN + DN). (See page 11, lines 8-12). Therefore, the Applicants submit that the term "integrated value of the difference value," as used in claim 1, is definite. The Applicants submit that the similar language in claims 3, 5, 6, 7, 11, and 23 is likewise definite.

C. "end of a counting period" & "start of a succeeding counting period"

The Applicants submit that the terms "end of a counting period" and "start of a succeeding counting period" are definite as used in claim 1. As described above, claim 1 corresponds to a first embodiment, which is depicted in Figures 2 and 3. Further, claim 1 recites "obtaining a count value by counting the number of effective transition

edges of the output clock signal during a counting period corresponding to the High level period of the reference clock signal." Thus, the counting period corresponds to the High level period of the reference clock signal, shown as T1 and T2 in Figure 3. Accordingly, the "end of a counting period" is the time at which the reference clock signal changes to a low level in the counting period, or the end of a high level period. The "start of a succeeding counting period" describes the next high level period.

Consistent with the claim language, Figure 3 shows the start of a succeeding counting period to T1 is the start of the next high level period, T2, following T1. The Applicants submit that this claim language is definite. The Applicants submit that the similar language in claims 3, 5, 6, 7, 11, and 23 is likewise definite.

D. Language in Claim 3

The Applicants note that the term "certain" has been removed from claim 3. In addition, "of the reference clock signal" has been inserted after the terms high or low period to clarify to what the high or low period corresponds. As described above for claim 1, the end of a high level period is the point at which the reference clock signal changes to a low level. The start of the succeeding low level period is the start of the next low level period.

The subject matter of claim 3 corresponds to an embodiment shown in Figure 5. Using the count value, CN1, obtained by counting the output clock signal for the High level period, T1, of the reference clock signal, SR, the difference value, DN1, integrated value, IN1, and analog control voltage, AV1, are generated in order. Based on this analog control voltage, AV1, the frequency of the output clock signal, ST, to be outputted by VCO7 is changed.

Using the count value CN2 obtained by counting the output clock signal for the low level period, T2, of the reference clock signal, SR, the difference value DN2, integrated value, IN2, and analog control voltage, AV2, are generated in order. Based on this analog control voltage, the frequency of the output clock signal, ST, to be outputted by VCO7 is changed.

The counter, 2, subtracter, 3, control voltage generation circuits, 3 and 4, and VCO7 provide the count value CN1, difference value, DN1, integrated value, IN1, and analog control voltage, AV1, in order within the low level period, T2, of the reference clock signal, SR, which is defined from the end of the High level period, T1, to the start of the next High level period, T3. Then, the frequency of the output clock signal ST is changed based on the analog control voltage, AV1. In this way, the structure defined in claim 3 can attain a good response.

Similarly, the counter, 2, subtracter, 3, control voltage generation circuits, 3 and 4, and VCO7 provide the count value CN2, difference value DN2, integrated value IN2, and analog control voltage AV2 in order within the High level period T3 of the reference clock signal SR, which is defined between the end of the Low level period T2 of the reference clock signal, SR, and the start of the next low level period T4. Further, the frequency of the output clock signal, ST, is changed based on the analog control voltage AV2. In this way, the structure defined in claim 3 can attain a good response time. If the response is low (slow), as can be seen in Figure 5, the timing when the analog control voltage changes a value AV2 is delayed to fall within the Low level period T4 of the reference clock signal, exerting an influence on a count value CN4 obtained at the counter 2.

Thus, the Applicants submit that the invention in claim 3 is clearly defined.

E. Claim 5

The Examiner cited the language "wherein the counter delivers the count value after the end of the counting period and in synchronization with the output clock signal" as misdescriptive because the Examiner asserts that the counter delivers the count value during the counting period and after the end of the counting period, the counter stops counting. If the Examiner's comments mean that the counter 2 outputs the count value CN1 in the form of a value (e.g. 0 to CN1) gradually incremented every time the output clock signal ST is inputted, this statement is incorrect. Instead, the counter, 2, continuously outputs a fixed value as the count value (e.g. CN1) until this is changed to the next count value (e.g. CN2). This is consistent with both the language of claim 5 and the specification. With reference to Figure 3, the counter outputs the count value CN (CN1, CN2) in sync with the output clock signal ST after the termination of the counting period (e.g. the High level period T1, T2 in the embodiment shown in Figure 3). More particularly, the counter outputs the count values CN1, CN2 in sync with the rising edge of the output clock signal ST. The specification describes this feature on page 10, lines 20-29. Note that claim 5 is not limited to the embodiment depicted in Figure 3, but covers the embodiments shown in Figures 3, 4, and 5.

If, as suggested by the Examiner, the count value repeatedly, continuously changed from 0 to CN1 during one counting period, the frequency of the output clock signal outputted from VCO would also change during one counting period and, thus, be periodically repeated. Such a configuration is completely different than the structure

intended by the present invention, as described in both the specification and claim 5. Therefore, the Applicants submit that claim 5 is not misdescriptive of the invention.

F. Claim 6

The Examiner cited "the counter counts each rising edge . . . and each falling edge as the effective transition edges of the output clock signal" as being misdescriptive. The Examiner points to Figure 3 and the specification on page 10, first paragraph as teaching that the counter counts a clock signal based only on the rising edge of the clock signal. The Examiner asserts that the counter cannot count a clock signal based on both rising and falling edges of the clock signal. However, claim 6 does not correspond to the embodiment shown in figure 3. Rather, claim 6 corresponds to a third example shown in Figure 7. Figure 6 is a similar type of depiction to claim 7 for the case where only the rising edges are counted. (See heading for Figures 6 and 7and page 19 line 6 to page 23 line 13). Figure 7 shows the case of counting at both a rising edge and a falling edge, as explained on page 20 at lines 18-20. Thus, the Applicants submit that the cited language is not misdescriptive.

The Examiner asserts that the term "effective transition edges of the output clock signal" is unclear. The Applicants respectfully disagree. The effective transition edge is clearly defined in the specification on page 5, lines 7-21.

G. Claims 8-10

The Examiner asserted that claims 8-10 are indefinite because of the deficiencies of claim 7. As the Applicant understands, claim 7 is being held indefinite for terms which are identical to those cited for claim 1. The Applicants respectfully traverse

this rejection for similar reasons to those discussed above for claim 1 and submit that claims 7-10 are definite.

II. Rejection under 35 U.S.C. § 102(b)

The Examiner rejected claims 1, 3, and 4-12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,928,208 to Kokubo et al. ("Kokubo"). The Examiner did not state that claim 23 was rejected as being anticipated by Kokubo. However, the Applicants assume this was a mistake as the rejection includes a description of Kokubo's teachings in reference to claim 23. The Applicants hereby traverse the rejection as follows.

Claim 5 was listed as being rejected as anticipated by Kokubo on page 3 under the citation of 35 U.S.C. § 102(b), however, there is no description of how claim 5 is anticipated by the cited art. As claim 5 is described in the Allowable Subject Matter section as distinguishing the cited art, we assume that claim 5 is not rejected under 35 U.S.C. § 102(b).

A. Claim 1

Applicants' invention, as set forth in claim 1, is directed to a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit including a counter for delivering the count value by counting the number of effective transition edges of the output clock signal existing during the counting period when the reference clock signal is only at a High level and the frequency of the output clock signal is changed during a period in which the clock signal is at low level, after the end of the counting period and before the start of a succeeding counting period.

The invention, as claimed in claim 1, allows the frequency clock signal to be maintained at a particular frequency during the next counting period, which suppresses jitter.

In contrast, Kokubo teaches, as shown in Figures 4 and 11, that one entire cycle of Low level and High level of an input clock signal is determined as a counting period A. Thus, Kokubo does not disclose or suggest at least the feature of counting the number of effective transition edges of the output clock signal existing during the counting period when the reference clock signal is *only* at a High level, as in claim 1.

Further, Kokubo shows the end of the counting period A coincides with the start of the succeeding counting period and the succeeding counting period starts just after the prior counting period. At column 3, lines 19-22, Kokubo teaches that the counter, 5, is reset to 0 and counting is restarted stating that the counter "then, resets to zero and beings counting again." Also, Figure 4 clearly shows that in a line, the count value counted by the counter, 5, reaches Nv and immediately changes to 1, and then increases again. Thus, Kokubo teaches the next counting period beginning just after the end of the prior counting period.

Further in contrast to claim 1, Kokubo teaches changing the frequency of the output clock signal during the next counting period. Claim 1 claims the frequency of the output clock signal changing during a period in which the reference clock signal is a Low level, after the end of the counting period and before the start of a succeeding counting period. In Kokubo, the count value Nv is output after the end of the counting period during the next counting period. (See Kokubo Figure 11). Therefore, a new analog control voltage Vr is generated based on a new count value after the end of the

counting period. The output clock signal of a new frequency obtained from VCO1 is after the end of the first counting period. At this time, as shown in Figure 4 of Kokubo, the next counting period has already begun.

Kokubo cannot suppress jitter as the invention of claim 1 can, because Kokubo changes the frequency of the output clock during the next counting period.

The Examiner asserted that Figure 4 shows that when the reference clock signal (fref) is a Low level, the count Nv changes thus, the output clock signal changes." However, the succeeding counting period in Kokubo already began after the reference clock signal (fref) changed to a Low level. Thus, the clock multiplication circuit described in Kokubo does not change the frequency of the output clock signal before the start of the next counting period.

Thus, the Applicants submit that Kokubo does not disclose or suggest at least the features of a counter for delivering the count value by counting the number of effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a High level and the frequency of the output clock signal is changed during a period in which the reference clock signal is a Low level, after the end of the counting period and before the start of a succeeding counting period.

For at least these reasons, the Applicants submit that claim 1 is allowable over the cited art.

B. Claim 3

The Applicants' invention as set forth in claim 3 is directed to a clock multiplication circuit including in part a counter for obtaining the count value at the end

of each High level period and each Low level period of the reference clock signal, in which when the count value obtained by counting during a High level period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal, and similar for when the count value is obtained during a Low level period.

In contrast, in Kokubo, one counting period (shown as B in Figure 4 of Kokubo), is an entire cycle of the reference clock signal fref (A), including both a High and Low level period of the reference clock signal. The count value, Nv is obtained only once during the continuous High and Low level period, as shown in (C). Thus, Kokubo fails to disclose or suggest a counter for obtaining the count value at the end of each High level period and each Low level period of the reference clock signal, as claimed in claim 3.

IN addition, claim 3 defines the response of the counter, subtracter, accumulator, DA conversion circuit, and the VCO to performing this change before the start of the next counting period. Claim 3 is directed to an embodiment of the invention which is depicted in Figure 5. Figure 5 of the present invention shows the number of effective transition edges of the output clock signal ST counted during the High level period, T1, of the reference clock signal, SR. After the end of T1 of this High level period, the count value CN1, difference value DN1, integrated value IN1, and analog control voltage AV1 are generated, changing the frequency of the output clock signal ST.

Similar to claim 3, Figure 5 also shows AV2, based on count value CN2 during the low period, changes the frequency of the output clock signal before the start of the next low period. Accordingly, the frequency of the output clock signal is controlled twice every one cycle of the reference clock signal. With the invention in claim 3, it becomes possible to suppress jitter even more effectively than in the inventions described in claims 1 and 23.

As discussed above, Kokubo teaches an entire cycle, both the high level and the low level of the reference signal as the counting period. The output clock signal is changed during the next counting period. Thus, Kokubo also fails to disclose or suggest when the count value obtained by counting during a High level period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal, and similar for when the count value is obtained during a Low level period.

Therefore, the Applicants submit that Kokubo does not disclose or suggest a clock multiplication circuit with at least the feature of a counter for obtaining the count value at the end of each High level period and each Low level period of the reference clock signal and when the count value obtained by counting during a High level period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock

signal, and similar for when the count value is obtained during a Low level period, as claimed in claim 3.

For at least this reason, the Applicants submit that claim 3 is allowable over the cited art.

C. Claims 6-10

The Examiner points to Kokubo Figure 8 in rejecting claims 6-9. Figure 8 of Kokubo is a circuit diagram of a lowpass filter, 4, in the clock multiplication circuit in the third embodiment, as described in Kokubo at column 6, lines 32-67 and in the brief description of the drawings. The lowpass filter, 4, is arranged to change its characteristics by the switching of switches SW3 and SW4 as shown in Figures 9 and 10 of Kokubo. Claims 6-9 of the present invention are unrelated to a lowpass filter. Thus, the Applicants submit that the teachings of the lowpass filter in Figure 8 of Kokubo, including switches SW3 and SW4 for simple switching do not teach elements of the inventions claimed in claims 6-9.

i. Claim 6

The Applicants' invention as set forth in claim 6 is directed to a clock multiplication circuit including, in part, a counter that counts each rising edge at which the output clock signal transmits from a Low level to a High level and each falling edge at which the output clock signal transmits from the High level to the Low level as the effective transition edge of the output clock signal.

Claim 6 is directed to an embodiment which is depicted in Figure 7. A separate embodiment is shown in Figure 6, where only the rising edges are counted. Counting merely the rising edge, as depicted in Figure 6, gives a count value of n/2. Variations

between cases A and B may occur and variations in the output clock signal will exist in about ±1 cycle in the cycle of the output clock signal. In contrast, when the counter counts both the rising edge and the falling edge of the output clock signal, as claimed in claim 6, the count value reaches n. Variations between cases A and B may occur and variations in the output clock signal will only exist in about ±0.5 cycle in the cycle of the output clock signal. In other words, when both the rising and falling edges are counted, as claimed in claim 6, variations included in the count value can be reduced by one half.

In contrast to claim 6, Kokubo teaches only that a falling transition of the output clock signal is counted. See Kokubo at column 3, lines 3-17. Thus, the Applicants submit that Kokubo does not disclose or suggest at least the feature of a counter that counts each rising edge at which the output clock signal transmits from a Low level to a High level and each falling edge at which the output clock signal transmits from the High level to the Low level as the effective transition edge of the output clock signal.

The Examiner asserts that Kokubo's counter counts the frequency of the output clock that includes low and high level or in other word, falling/rising edges. The Applicants respectfully traverse this argument. The counter, 5, of the present invention does not count the frequency of the output clock signal, it merely counts the number of the falling edges and/or the rising edges of the output clock signal appearing within a certain period. The counter can be configured to count only the falling edges, only the rising edges, or both of the falling edges and the rising edges, or to count the falling edges on alternate falling edges (incrementing the count value by 1 upon every detection of two falling edges). If all the falling edges of the output clock signal appearing within the counting period are counted, the value becomes equal to the

number of cycles of the output clock signal generated during that counting period. It appears that this is what the Examiner regards as "counting the frequency" by Kokubo.

However, claim 6 is directed to a counter that counts each rising edge at which the output clock signal transmits from a Low level to a High level and each falling edge at which the output clock signal transmits from the High level to the Low level as the effective transition edge of the output clock signal. When both the falling edges and the rising edges are counted, the count value should be double the number of cycles of the output clock signal generated during that counting period. This value differs from the number of cycles of the output clock signal or "frequency" indicated by the Examiner. As described above, the configuration claimed in claim 6 reduces variations in the count value by half.

Thus, the Applicants submit that Kokubo does not disclose or suggest at least the feature of a counter that counts each rising edge at which the output clock signal transmits from a Low level to a High level and each falling edge at which the output clock signal transmits from the High level to the Low level as the effective transition edge of the output clock signal.

For at least this reason, the Applicants submit that claim 6 is allowable over the cited art.

ii. Claims 7-10

The Applicants' invention as set forth in claim 7 is directed to a clock multiplication circuit including, in part, a multiplier for multiplying the difference value by a predetermined factor and delivering a multiplied difference value to the control voltage

generation circuit that is interposed between the subtracter and the control voltage generation circuit.

The Examiner asserts that Kokubo's element 18 is a multiplier and that the factor of the multiplier depends on bits of a subtracter. The Applicants respectfully traverse this rejection. Kokubo merely explains the procedure of calculating a difference value and an integrated value, the same as disclosed in the first embodiment of the present application and claimed in claim 1. Claim 7 is directed to a modified embodiment.

Kokubo teaches the count value Nv outputted by the counter, 5, subtracted from a predetermined value, N, stored in a memory device, 6, to output a difference value (=N-Nv). (See Kokubo at column 7, lines 4-11). An accumulator register, 18, sums "all bits" of the difference value and the existing contents in the accumulator register. The resultant sum is regarded as the existing content of the accumulator register, 18. In other words, assuming that the difference value is dn and the existing contents of the accumulator register is acn, the existing contents is set at acn=acn +dn. (It appears that Kokubo used the expression "all bits" to clarify a difference from changing of part of bits in the register, as in the first embodiment of Kokubo.)

Similarly, in the first embodiment described in the specification of the present application, the subtracter, 3, outputs a difference value DN(=BN-CN) by subtracting a count value, CN, from a reference value, BN, stored therein. Then, the integrator (similar to the accumulator in Kokubo) generates a new integrated value by adding the difference value to the previous integrated value stored therein (IN=IN+DN).

Thus, the predetermined value N in Kokubo corresponds to the reference value BN in the present application, the count value Nv corresponds to the present count

value CN, and the existing contents of the accumulator register, acn, corresponds to the integrated value IN of the present invention and related calculations are made. (See page 10 line 30 to page 11 line 17).

The embodiment taught by Kokubo and the first embodiment of the present application are different than the invention of claim 7, which further includes a multiplier for multiplying the difference value by a predetermined factor.

The accumulator of Kokubo is merely a device for adding, as suggested by its name and as described in column 7, lines 4-11. Therefore, the Applicants submit that Kokubo does not disclose or suggest a clock multiplication circuit comprising at least the feature of a multiplier for multiplying the difference value by a predetermined factor and delivering a multiplied difference value to the control voltage generation circuit that is interposed between the subtracter and the control voltage generation circuit.

For at least this reason, the Applicants submit that claim 7 is allowable over the cited art. As claim 7 is allowable, the Applicants submit that claims 8-10, which depend from allowable claim 7, are likewise allowable.

The Applicants submit that claim 10 is further distinguished by the feature of control factor means for controlling the factor of the multiplier . . . . As discussed above, Kokubo does not disclose or suggest a multiplier. Thus, Kokubo does not teach control factor means for controlling the factor of a multiplier.

The Examiner cites Figure 8 of Kokubo in relation to claim 10 of the present invention. However, as discussed above, Figure 8 shows a lowpass filter arranged with the use of switches. Furthermore, Kokubo teaches the lowpass filter, 4, located just

before VCO1 and behind DAC9 (further behind switches SW1 and SW2). (See figures 2, 7, and 11 of Kokubo).

In contrast, the factor control means in claim 10 is arranged to control the factor of the multiplier which "is interposed between the subtracter and the control voltage generation circuit" as claimed in claim 7, from which claim 10 depends. The means pointed to in Kokubo would be ineffective even if it were disposed at the lowpass filter because the lowpass filter is not arranged to fix the factor of a multiplier.

Thus, the Applicants submit that claim 10 is further allowable over the cited art for at least these reasons.

D. Claims 11-12

The Applicants' invention as set forth in claim 11 is directed to a clock multiplication circuit including, in part, a subtracter for delivering a difference value obtained by subtracting either the count value or a subtracter reference value from the other wherein the subtracter is capable of switching the subtracter reference value. Claim 11 is directed to an embodiment of the invention which is depicted in Figures 11 to 14 of the present application.

The Examiner asserts that in Kokubo controller 10 initializes the "multiplier" with different digital data, citing column 3, lines 60-64 of Kokubo. However, claim 11 is defined such that a reference value in the subtracter, BN in the specification, is changeable, which is not the same as the section cited in Kokubo.

The Examiner pointed out that a subtracter, 11, in Kokubo can change a reference value, N. However, 11 shown in Figure 11 of Kokubo represents an internal

counter in a controller which counts the number of cycles of the input clock signal fref. This internal counter is not a subtracter.

Furthermore, the section cited by the Examiner, column 7, lines 22-29 of Kokubo, merely teach that the fourth embodiment of Kokubo is effective in the case where the frequency of the input clock signal is low and the reference value, N, is large. Kokubo does not teach changing of the reference value, N.

Thus, the Applicants submit that Kokubo does not teach or suggest a clock multiplication circuit comprising at least a subtracter for delivering a difference value obtained by subtracting either the count value or a subtracter reference value from the other wherein the subtracter is capable of switching the subtracter reference value.

For at least these reasons, the Applicants submit that claim 11 is allowable over the cited art.

As claim 11 is allowable, the Applicants submit that claim 12, which depends from allowable claim 11, is likewise allowable.

Further regarding claim 12, the Examiner asserted that the claimed storage means for storing the reference value reads on element 11 of Kokubo. As mentioned above, however, the internal counter, 11, of Kokubo is the internal counter of the controller, 10, to count the number of cycles of the input clock signal fref. Thus, the internal counter 11 of Kokubo is not the storage means for storing the reference value of claim 12.

The Applicants do not dispute that memory device, 6, of Kokubo stores a reference value, N. However, claim 12 is directed to storage means configured so as to enable the subtracter reference value to be stored in the reference value storage means

from outside. Kokubo does not disclose or suggest a clock multiplier configured in a finished state to enable changing of the reference value N stored in the memory device.

Thus, the Applicants submit that claim 12 further distinguishes Kokubo in claiming reference value storage means configured so as to enable the subtracter reference value to be stored in the reference value storage from outside.

E. Claim 23

The Applicants' invention as set forth in claim 23 is directed to a clock multiplication circuit including, in part, a counter for delivering a count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a low level and the frequency of the output clock signal is changed during a period in which the reference clock signal is a High level, after the end of the counting period and before the start of a succeeding counting period.

Claim 23 is directed to an invention that can be generalized as a reverse of claim 1. Claim 23 is directed to an embodiment of the invention depicted in Figure 4. Claim 23 requires that the counting period exist only when the reference clock signal is at a low level and the output clock signal is changed when the reference clock signal is at a high level (between counting periods), whereas claim 1 requires that the counting period exist only during a high level and the output clock signal is changed only during a low level (between counting periods).

As discussed above for claim 1, Kukobo teaches both the high and low levels as counting periods and the output clock signal being changed during a counting period.

Thus, the Applicants submit, for reasons similar to those discussed above for claim 1, that Kukobo fails to disclose or suggest a clock multiplication circuit including at least the features of a counter for delivering a count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a low level and the frequency of the output clock signal is changed during a period in which the reference clock signal is a High level, after the end of the counting period and before the start of a succeeding counting period, as claimed in claim 23.

For at least this reason, the Applicants submit that claim 23 is allowable over the cited art.

CONCLUSION

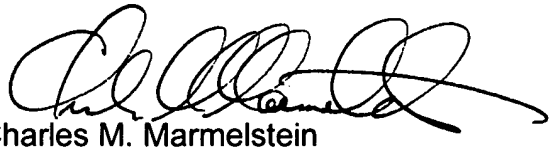
For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, with reference to Attorney Docket No. 024016-00063

Respectfully submitted,

Arent Fox PLLC



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